2823

PATENT APPLICATION

#8/ AMDT A 11/8/02 VA

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Docket No: Q62494

Ryo KUBOTO, et al.

Appln. No.: 09/817,233

Group Art Unit: 2823

Confirmation No.: 8072

Examiner: Hsien Ming LEE

Filed: March 27, 2001

For: MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE HAVING DRAM CAPACITORS

AMENDMENT UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action dated June 28, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 8, 10 and 11 without prejudice or disclaimer.

Please enter the following amended claims:

1. (Amended) A method of manufacturing a system-on-chip semiconductor device, including a CMOS logic circuit and a DRAM on the same semiconductor chip, comprising the steps of:

providing a CMOSlogic circuit portion and a DRAM portion of a substrate;

forming a first transistor on said substrate at said CMOS logic circuit portion;

forming a second transistor on said substrate at said DRAM portion;